



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

YONEMARU, M.

Atty. Ref.: 829-618; Confirmation No. 3114

Appl. No. 10/720,764

TC/A.U. 2826

Filed: November 25, 2003

Examiner: Dickey, T.

For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS
TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS
CONNECTED IN SERIES

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October 17, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT

Responsive to the Official Action dated July 17, 2006, please amend the above-identified
application as follows: